In the Claims:

Please cancel claims 1 and 20-27 and amend the claims as indicated below. This listing of claims replaces all prior versions.

1. (canceled)

2. (currently amended) [[The]]A method ~~of claim 1, wherein~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die including ~~includes~~ applying an electric field to circuitry via a die passivation layer in a conventionally packaged semiconductor die;

detecting a response of the die to the applied electric field; and

using the response to detect an electrical characteristic from the die.

3. (currently amended) [[The]]A method ~~of claim 1, wherein~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die including ~~includes~~ applying an electric field to circuitry via a backside of a flip-chip packaged die;

detecting a response of the die to the applied electric field; and

using the response to detect an electrical characteristic from the die.

4. (original) The method of claim 3, wherein applying an electric field to circuitry via a backside of a flip-chip packaged die includes applying an electric field via a thinned backside of the flip-chip packaged die.

5. (original) The method of claim 4, further comprising thinning the backside of the flip-chip packaged die and thereby forming the thinned backside.

6. (currently amended) [[The]]A method ~~of claim 1, wherein~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die including~~includes~~ applying an electric field to circuitry via an insulator portion of silicon-on-insulator structure in a die;

detecting a response of the die to the applied electric field; and

using the response to detect an electrical characteristic from the die.

7. (original) The method of claim 6, further comprising thinning a portion of the die and exposing the insulator portion of the silicon-on-insulator structure, wherein applying an electric field to circuitry via the insulator portion includes applying the electric field via the exposed insulator portion.

8. (currently amended) [[The]]A method ~~of claim 1, wherein~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying ~~the~~an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die~~includes~~ using at least one of: a scanning probe microscope, an[[d]] atomic force microscope and a capacitance probe microscope;

detecting a response of the die to the applied electric field; and

using the response to detect an electrical characteristic from the die.

9. (currently amended) [[The]]A method ~~of claim 1, wherein~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die including

~~includes~~ positioning a probe tip over a portion of circuitry in the die and applying a voltage to the probe tip;

detecting a response of the die to the applied electric field; and

using the response to detect an electrical characteristic from the die.

10. (original) The method of claim 9, wherein applying a voltage to the probe tip includes applying a voltage that varies over time to the probe tip.

11. (original) The method of claim 9, wherein detecting a response of the die to the applied electric field includes detecting a position of the probe tip over the die and mapping the detected response to circuitry in the die below the probe tip.

12. (original) The method of claim 9, wherein positioning the probe tip includes scanning the probe tip over the die.

13. (original) The method of claim 12, wherein detecting a response of the die includes detecting responses from a plurality of circuits in the die as the probe tip is scanned over the circuits.

14. (original) The method of claim 9, wherein applying a voltage to the probe tip includes applying a periodic voltage that is relative to a voltage at a reference node in the die.

15. (currently amended) The method of claim 9, wherein positioning a probe tip includes positioning a probe tip having a radius that is sufficiently small to stimulate a selected node in the die without ~~necessarily~~ stimulating circuitry adjacent to the selected node.

16. (original) The method of claim 9, wherein positioning a tip over a portion of circuitry in the die includes positioning the tip using nanometer-level resolution.

17. (currently amended) [[The]]A method ~~of claim 1, wherein~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die including ~~includes~~ applying the electric field to circuitry via an opaque layer in the die, the circuitry being buried in the die below the opaque layer;

detecting a response of the die to the applied electric field; and

using the response to detect an electrical characteristic from the die.

18. (currently amended) [[The]]A method ~~of claim 1, further~~for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the method comprising:

applying an electric field to the die via a voltage-application tool, separate from the die and using the applied electric field to stimulate circuitry in the die;

detecting a response of the die to the applied electric field;

using the response to detect an electrical characteristic from the die; and

using the detected electrical characteristic to provide a modified die design and manufacturing a semiconductor device using the modified die design.

19. (original) A semiconductor device manufactured using the modified die design of claim 18.

20-27. (canceled)

28. (original) A system for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the system comprising:

means, separate from the die and adapted for applying an electric field to the die and using the applied electric field to stimulate circuitry in the die;

means for detecting a response of die to the applied electric field; and

means for using the response to detect an electrical characteristic of the die.

29. (original) A system for analyzing a semiconductor die having circuitry in a circuit side opposite a back side, the system comprising:

a probe tip arrangement, separate from the die and adapted for applying an electric field to the die for stimulating circuitry in the die;

electrical detection circuitry adapted for detecting a response of die to the applied electric field; and

a computer arrangement adapted for using the response to detect an electrical characteristic of the die.

30. (currently amended) The system of claim 29, wherein the probe tip is sufficiently small to apply an electric field to stimulate a selected circuit node in the die without ~~necessarily~~ stimulating surrounding circuitry in the die.